CLAIMS

1. A method for fabricating an integrated circuit comprising a nonvolatile memory comprising a nonvolatile memory cell comprising two floating gates, a select gate, and two control gates, the nonvolatile memory further comprising a first peripheral transistor, the method comprising:

(a) forming a dielectric layer on a semiconductor substrate, the dielectric layer comprising a first dielectric region ("select gate dielectric") and a second dielectric region ("first peripheral transistor gate dielectric"), wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed simultaneously;

(b) forming a first layer over the dielectric layer and patterning the first layer to provide (i) the select gate on the select gate dielectric, and (ii) a gate for the first peripheral transistor on the first peripheral transistor gate dielectric;

(c) after the operation (b), forming the floating gates and the control gates for the memory cell.

2. The method of Claim 1 wherein the memory cell comprises a channel region in the semiconductor substrate, the select gate controls a conductivity of a portion of the channel region, and each of the floating gates overlies a respective other portion of the channel region.

3. The method of Claim 2 wherein the control gates overlie the respective floating gates.

4. The method of Claim 1 wherein the operation (b) comprises forming a plurality of layers over the semiconductor substrate, wherein the floating gates and the control gates are formed from the plurality of layers.

5. The method of Claim 1 wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed by oxidation of the semiconductor substrate.

6. The method of Claim 5 wherein the select gate dielectric and the first peripheral transistor gate dielectric comprise silicon oxide.

7. The method of Claim 1 further comprising, after the operation (b), forming a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gates from the substrate, wherein the floating gate dielectric is formed of the same material as the select gate dielectric but is thinner than the select gate dielectric.

8. The method of Claim 1 further comprising forming a second peripheral transistor gate dielectric on the semiconductor substrate for a second peripheral transistor, and forming a gate of the second peripheral transistor on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric is made from the same material as the select gate dielectric and the first peripheral transistor gate dielectric but the thickness of the second peripheral transistor gate dielectric is different from the thickness of the first peripheral transistor gate dielectric.

9. The method of Claim 8 wherein the second peripheral transistor gate dielectric is thinner than the first peripheral transistor gate dielectric.

10. The method of Claim 8 wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in said memory.

11. The method of Claim 8 wherein the second peripheral transistor gate dielectric is formed after the start of the operation (a).

12. The method of Claim 8 wherein the second peripheral transistor gate dielectric is formed before the operation (b).

13. The method of Claim 8 wherein the gate of the second peripheral transistor is formed by patterning the first layer in the operation (b).

14. The method of Claim 1 wherein the memory cell is one of a plurality of nonvolatile memory cells of said memory, each memory cell comprising two floating gates, a select gate, and two control gates, wherein:

the operation (a) simultaneously forms select gate dielectric for each of the memory cells; and

the operation (b) simultaneously forms the select gate for each of the memory cells on the corresponding select gate dielectric.

15. The method of Claim 1 wherein during a memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation.

16. The method of Claim 15 wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory.

17. The method of Claim 1 wherein the memory is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates and a channel region of the memory cell, the channel region being located in the semiconductor substrate.

18. An integrated circuit comprising:

a semiconductor substrate;

a dielectric ("select gate dielectric") on the semiconductor substrate;

a select gate of a nonvolatile memory cell on the select gate dielectric;

two floating gates of the nonvolatile memory cell;

two control gates of the nonvolatile memory cell;

a first peripheral transistor for accessing the memory cell, the first peripheral transistor comprising:

a first peripheral transistor gate dielectric on the semiconductor substrate; and

a gate on the first peripheral transistor gate dielectric;

wherein the first peripheral transistor gate dielectric has the same thickness as the select gate dielectric.

19. The integrated circuit of Claim 18 wherein the semiconductor substrate comprises a channel region of the memory cell, wherein the select gate controls a conductivity of a portion of the channel region, and each of the floating gates overlies a respective other portion of the channel region.

20. The integrated circuit of Claim 19 wherein each of the control gates overlies a respective on of the floating gates.

21. The integrated circuit of Claim 18 wherein the semiconductor substrate is a silicon substrate, and the select gate dielectric and the first peripheral transistor gate dielectric comprise silicon oxide.

22. The integrated circuit of Claim 18 further comprising a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gates from the substrate, wherein the floating gate dielectric is made of the same material as the select gate dielectric but is thinner than the select gate dielectric.

23. The integrated circuit of Claim 18 further comprising a second peripheral transistor comprising a second peripheral transistor gate dielectric on the semiconductor substrate and a gate on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric is made of the same material as the select gate transistor gate dielectric and the first peripheral transistor gate dielectric but the thickness of the second peripheral transistor gate dielectric is different from the thickness of the first peripheral transistor gate dielectric.

24. The integrated circuit of Claim 23 wherein the second peripheral transistor gate dielectric is thinner than the first peripheral transistor gate dielectric.

25. The integrated circuit of Claim 23 wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in said memory.

26. The integrated circuit of Claim 18 wherein the memory cell is one of a plurality of nonvolatile memory cells of the integrated circuit, each memory cell comprising a dielectric ("select gate dielectric") on the semiconductor substrate, a select gate on the select gate dielectric, two floating gates, and two control gates;

wherein the select gate dielectric of each memory cell has the same thickness as the first peripheral transistor gate dielectric.

27. The integrated circuit of Claim 18 wherein during a memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation.

28. The integrated circuit of Claim 27 wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory.

29. The integrated circuit of Claim 18 wherein the memory cell is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates and a channel region of the memory cell, the channel region being located in the semiconductor substrate.